OIPE JC105
JUL 19 2004
PATENT & TRADEMARK OFFICE



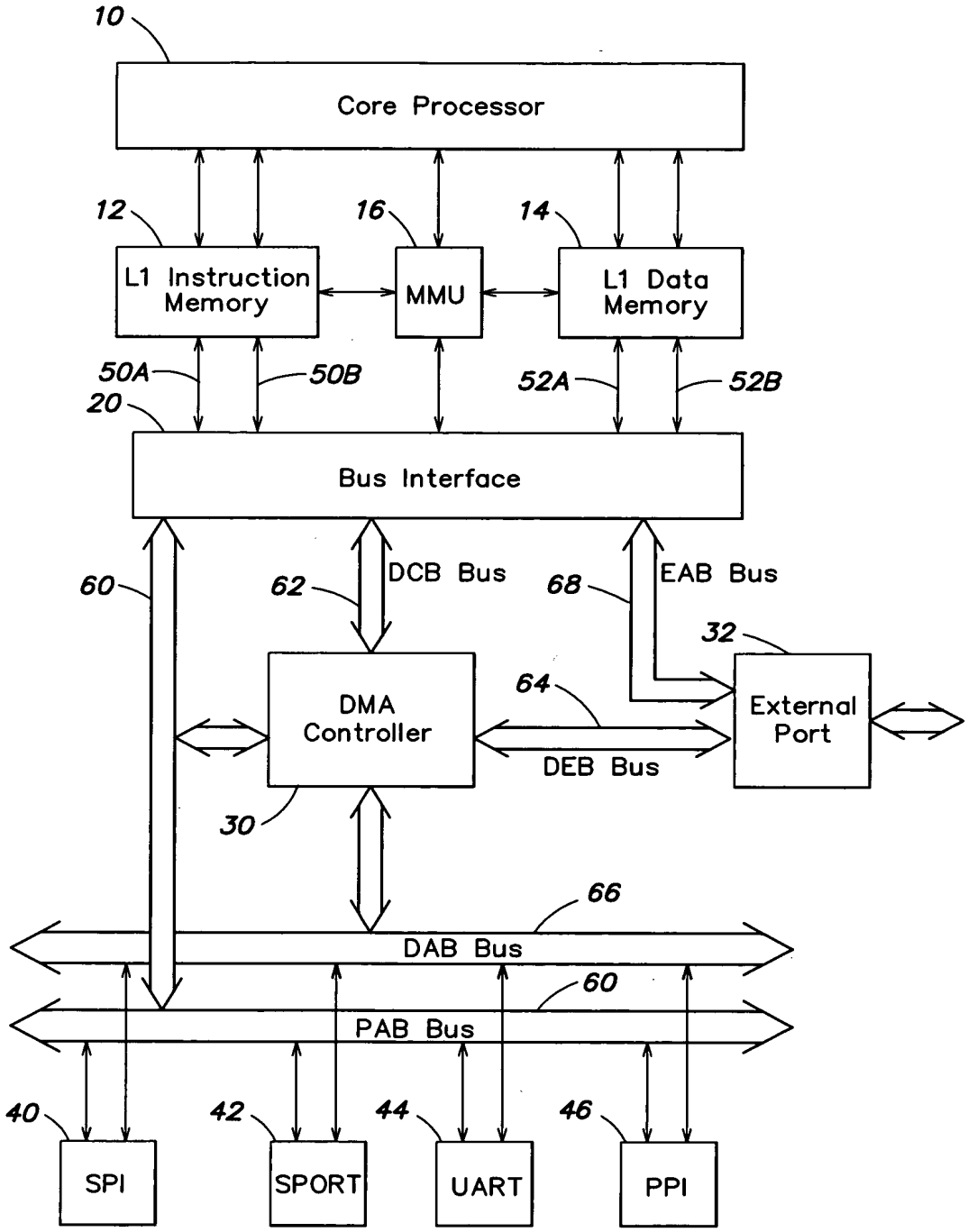


FIG. 1

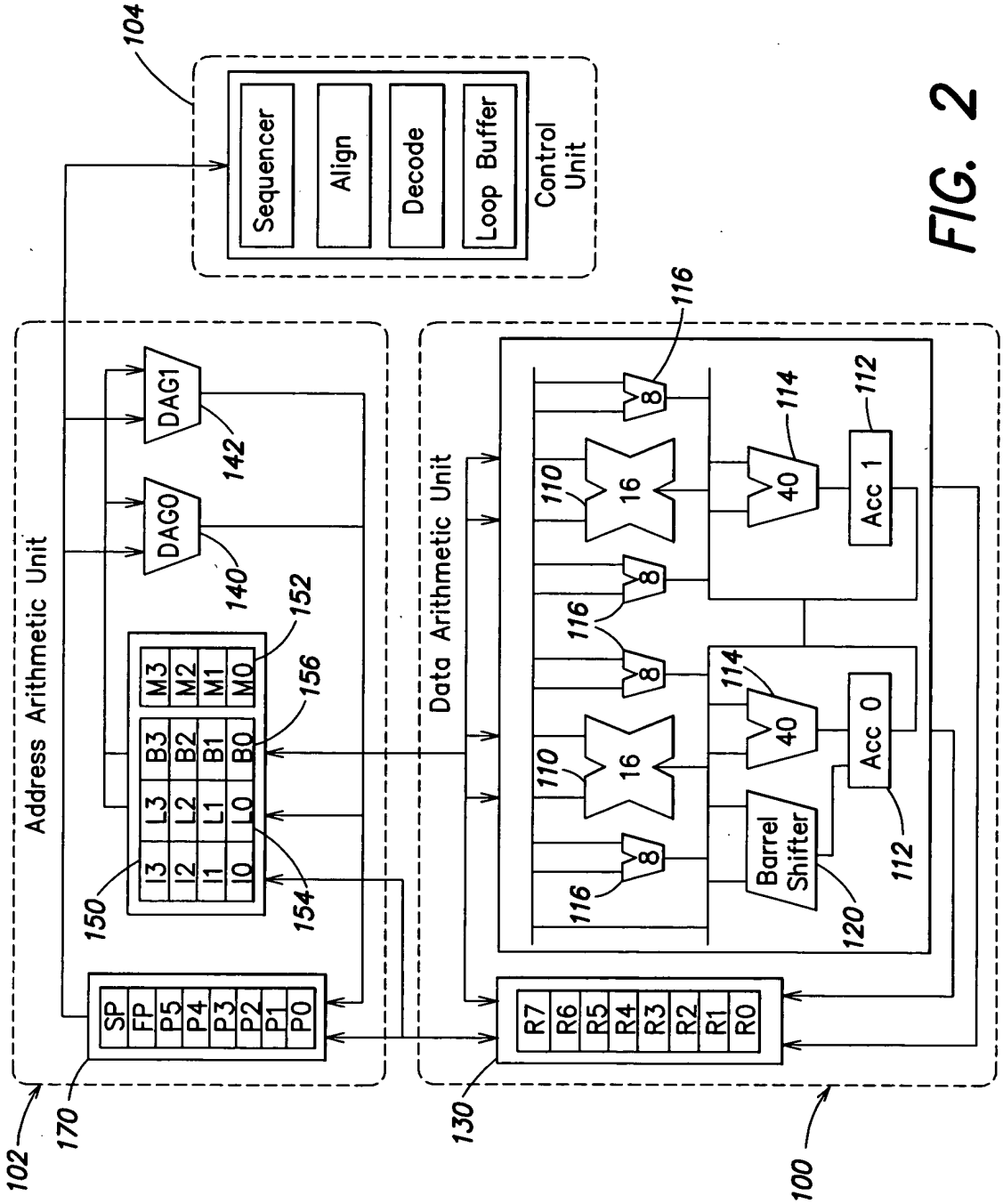
104
Sequencer
Align
Decode
Loop Buffer
Control Unit
Address Arithmetic Unit
Data Arithmetic Unit
DAG1
DAG0
142
140
152
156
154
150
M3
M2
M1
M0
B3
B2
B1
B0
L3
L2
L1
L0
I3
I2
I1
I0
SP
FP
P5
P4
P3
P2
P1
P0
R7
R6
R5
R4
R3
R2
R1
R0
116
110
16
114
40
112
Acc 1
Acc 0
Barrel Shifter
120
102
170
130
100

FIG. 2

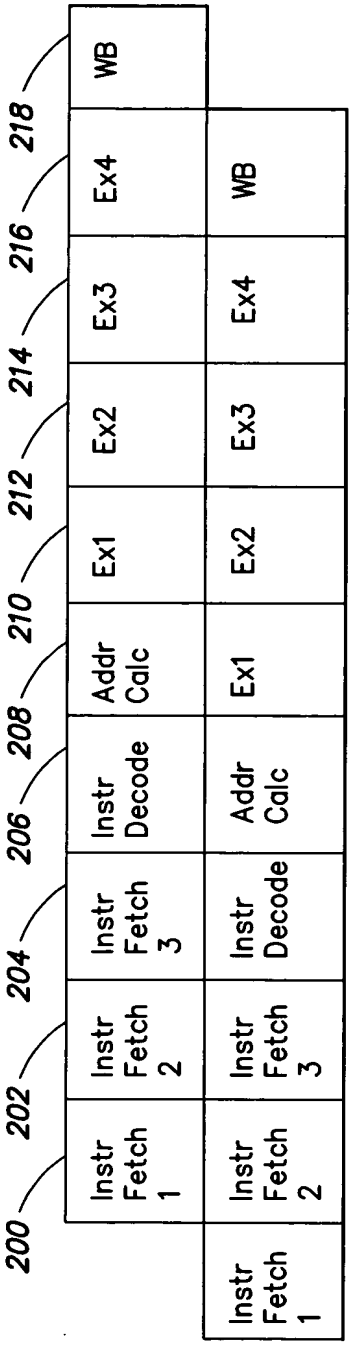
200
202
204
206
208
210
212
214
216
218
Instr Fetch 1
Instr Fetch 2
Instr Fetch 3
Instr Decode
Addr Calc
Ex1
Ex2
Ex3
Ex4
WB

FIG. 3

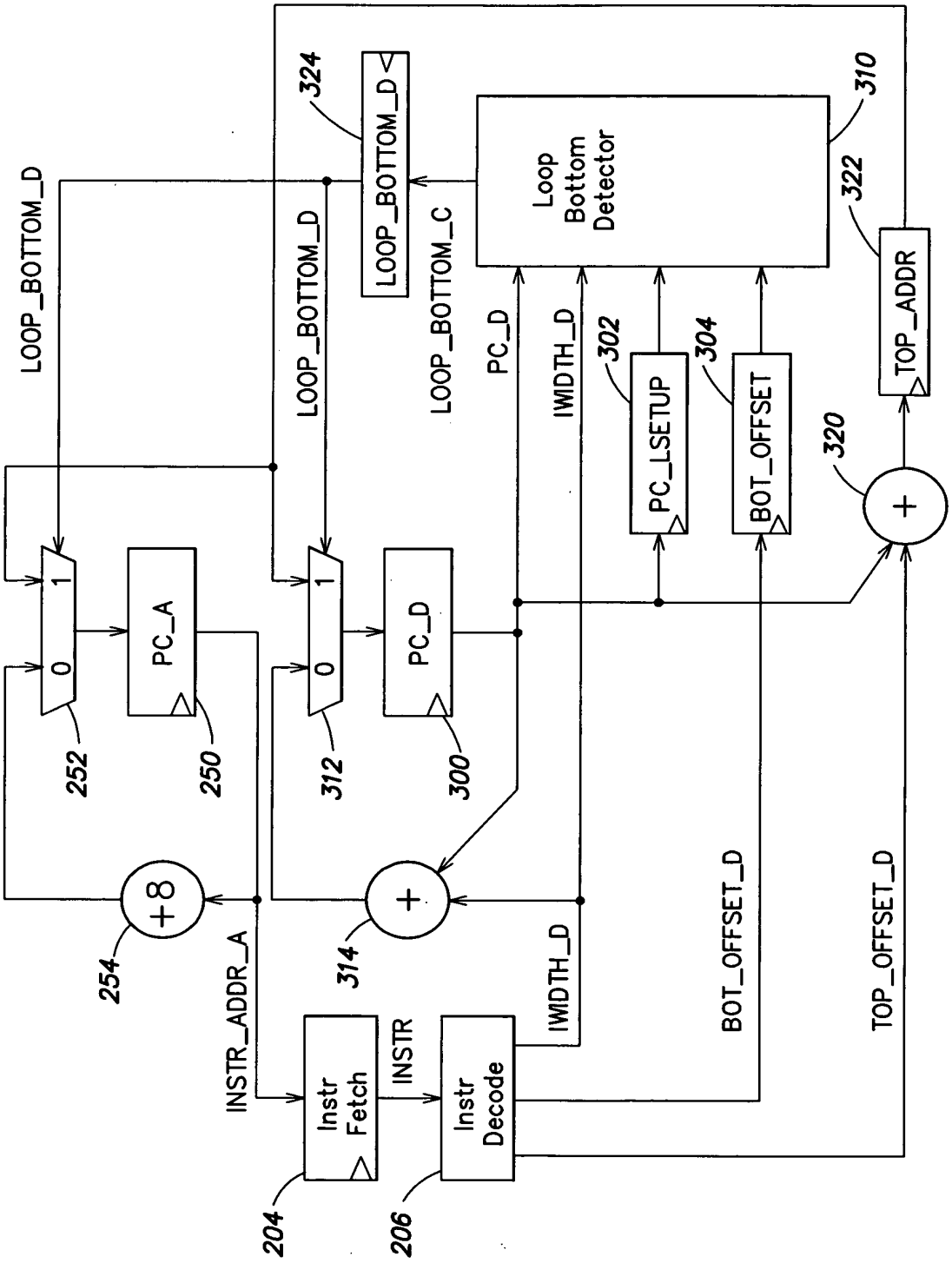
LOOP_BOTTOM_D
LOOP_BOTTOM_D
LOOP_BOTTOM_D
LOOP_BOTTOM_C
PC_D
IWIDTH_D
PC_LSETUP
BOT_OFFSET
TOP_ADDR
Loop Bottom Detector
324
310
322
302
304
320
PC_A
PC_D
252
250
312
300
+8
+
254
314
INSTR_ADDR_A
IWIDTH_D
BOT_OFFSET_D
TOP_OFFSET_D
Instr Fetch
INSTR
Instr Decode
204
206

FIG. 4

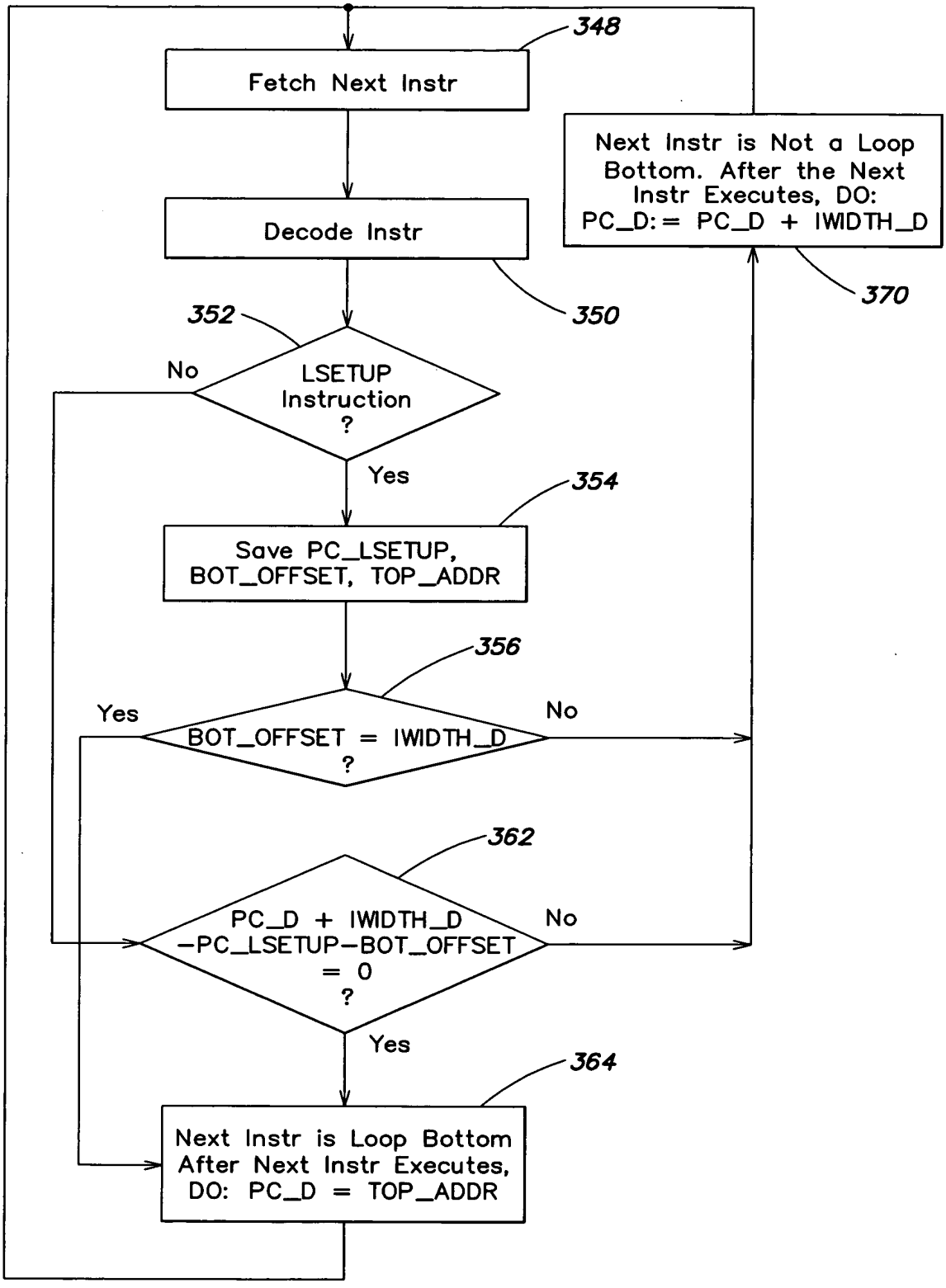
348
Fetch Next Instr
Decode Instr
350
Next Instr is Not a Loop Bottom. After the Next Instr Executes, DO: PC_D:= PC_D + IWIDTH_D
370
352
No
LSETUP Instruction ?
Yes
354
Save PC_LSETUP, BOT_OFFSET, TOP_ADDR
356
Yes
BOT_OFFSET = IWIDTH_D ?
No
362
PC_D + IWIDTH_D -PC_LSETUP-BOT_OFFSET = 0 ?
No
Yes
364
Next Instr is Loop Bottom After Next Instr Executes, DO: PC_D = TOP_ADDR

FIG. 5

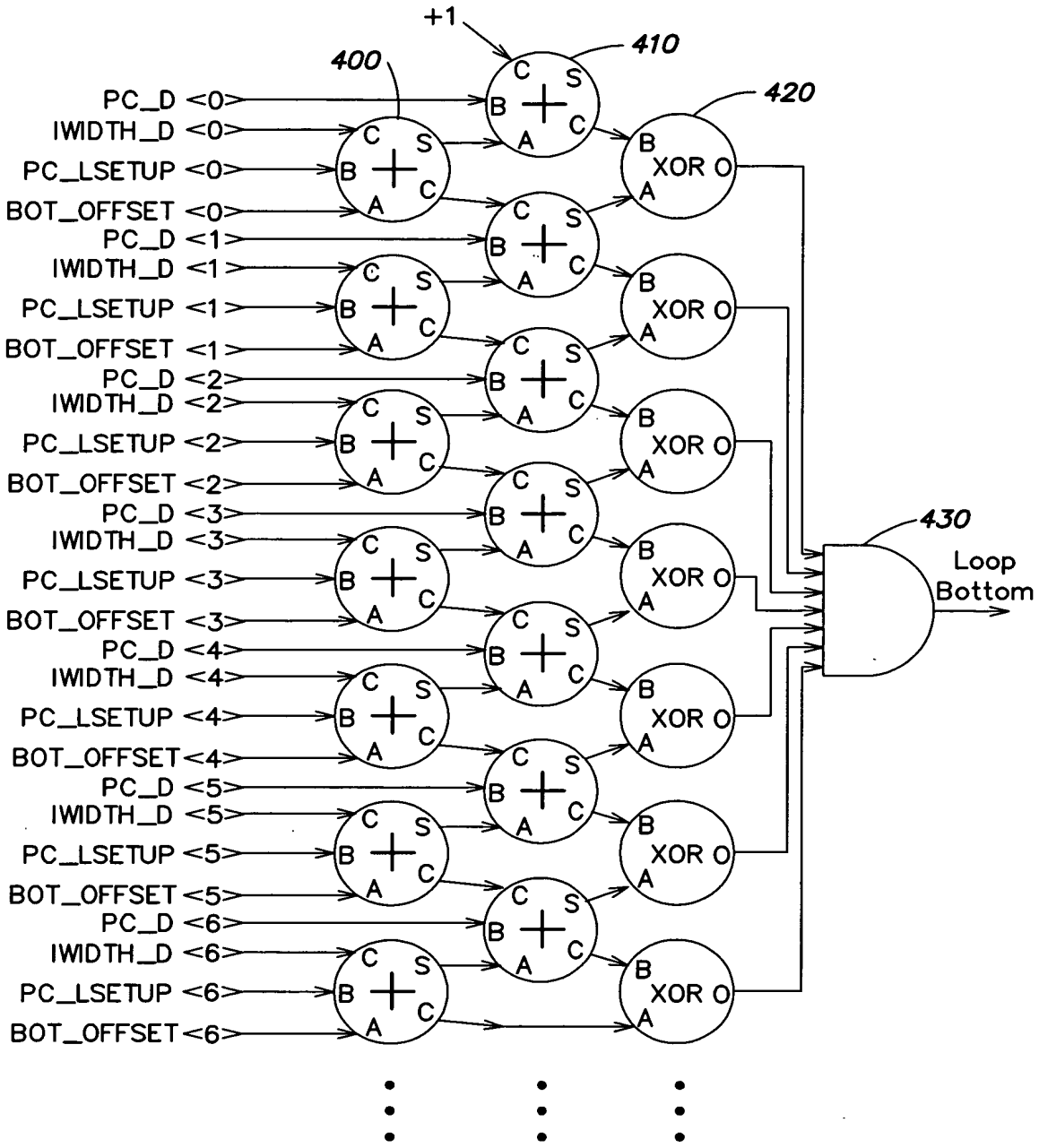
+1
400
410
420
430
PC_D <0>
IWIDTH_D <0>
PC_LSETUP <0>
BOT_OFFSET <0>
PC_D <1>
IWIDTH_D <1>
PC_LSETUP <1>
BOT_OFFSET <1>
PC_D <2>
IWIDTH_D <2>
PC_LSETUP <2>
BOT_OFFSET <2>
PC_D <3>
IWIDTH_D <3>
PC_LSETUP <3>
BOT_OFFSET <3>
PC_D <4>
IWIDTH_D <4>
PC_LSETUP <4>
BOT_OFFSET <4>
PC_D <5>
IWIDTH_D <5>
PC_LSETUP <5>
BOT_OFFSET <5>
PC_D <6>
IWIDTH_D <6>
PC_LSETUP <6>
BOT_OFFSET <6>
C S B + A C
B XOR O A
Loop
Bottom

FIG. 6